REMARKS

Applicant has amended pages 2, 5 and 13 of the specification as suggested by the Examiner to overcome the objection to the disclosure which should now be withdrawn.

The rejection of claims 1-18 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully traversed.

Claims 1 and 18 have been amended removing the wording which the Examiner considers to make no sense to read "each of the pulses having one of positive and negative polarities". In addition, the word "integrating" has been removed and the word "accumulating" substituted therefor so as to indicate a different function for the integrating means from that of a simple mathematical integration. Claim 18 has been amended in a similar fashion to that of claim 1. In claim 2, the last two lines have been amended to read:

"During a period of supply of said input pulse signal having the other of said polarities no chattering is generated in the input pulse signal during the period."

This should overcome the problem regarding the lack of understanding of the meaning of the wording in claim 2.

Claims 3 and 6 have been amended as suggested by the Examiner. Accordingly, the rejection of claims 1 to 18 under 35 USC 112, second paragraph, should now be withdrawn.

The Abstract has been revised to conform to the changes in the claims and a new Abstract provided.

The rejection of claims 1, 2, 8 and 18 under 35 USC 102(e) as being anticipated by either Crofts, et al or Tamayama is respectfully traversed. Crofts, et al discloses an oscillator having a waveform generating technique. In order to generate an accurate signal with a predetermined frequency output, a switching capacitor circuit independent of the resistor circuit which sets the frequency of the oscillator is used so that an offset voltage on a signal output from an operational amplifier is compensated by the switching capacitor circuit, thereby eliminating (filtering) oscillation components of the output signal of the operational amplifier.

The Tamayama reference discloses a signal reading technique for a solid-state image sensing device. In order to reduce noise contained in an image sensing signal output from a CCD, a feed through signal component representing a reference level of the video signal and the video signal component are extracted by using two gate circuits. A differential signal between the two signal components is integrated and an integration coefficient of an integrating circuit is controlled in accordance with a control signal.

In contradistinction, the present invention relates to a signal processing circuit for obtaining an output signal corresponding to a pulse width of an input signal with the circuit comprising means for accumulating the pulse widths of the input pulse signal for a predetermined period of time with each of the pulses having one of positive

and negative polarities and outputting means for outputting the output signal corresponding to the accumulated pulse widths. There is no counterpart in either of the cited references to the signal processing circuit as now claimed in claim 1 or in claim 18. Accordingly, the rejection under 35 USC 102 should be withdrawn.

It seems that the Examiner may have cited the Crofts, et al reference based on the assumption that the switched capacitor circuit of the Crofts, et al reference corresponds to the charge circuit for accumulating the pulse widths according to the present invention. The Crofts, et al reference may have an objective common to the present invention to reduce noise components in the output signal but the technical field to which the Crofts, et al reference matter relates is completely different from that of the present invention. Accordingly, the Crofts, et al reference does not teach the following as is disclosed in the subject application:

1) Outputting an output signal corresponding to the pulse width of the input signals;

2) Accumulating pulse widths of the input pulse signals for a predetermined period with each pulse width having one of positive and negative polarities;

3) Outputting an output signal corresponding to the accumulated pulse widths.

Moreover, the references do not teach the following:

Sample-holding a charge voltage accumulated in accordance with one of the polarities during a period of the other polarity to avoid chattering of the input pulse signal.

It should further be noted that the word "integrate" in the present invention is not intended to simply mean a mathematical integration but rather a step of accumulation and as such, the word "accumulate" has been substituted for the word "integrate" in the claims and in the Abstract.

Applicant acknowledges that claims 3-7 and 9-17 would be allowable if rewritten to overcome the rejections under 35 USC 112, second paragraph. Accordingly, these claims should now be allowable relative to the rejection under 35 USC 112.

Reconsideration and allowance of claims 1-18 is respectfully solicited.

Respectfully submitted,

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focus/tracking servo circuit 50, a feed servo circuit 51, a spindle servo circuit 52, a CD encode/decode circuit 53, a D/A converter 54, an audio amplifier 55, RAMs 56 and 58, a CD-ROM encode/decode circuit 57, an interface/buffer controller 59, and a CPU 60. The optical disk device 100 records/reproduces information according to commands transmitted from a host computer 61.

The spindle motor 42 is driven by the spindle servo circuit 52 so as to revolve the disk 40 at a predetermined revolving speed. The optical system 41 is arranged opposite the disk 40. The optical system 41 projects a laser light on the disk 40 so as to record information on the disk 40. The optical system 41 also receives a light reflected ~~on~~ from the disk 40 so as to output a reproduction signal corresponding to information recorded on the disk 40. The optical system 41 is controlled by the sled motor 43 and the focus/tracking servo circuit 50 so as to project a light beam at a predetermined position B on the disk 40.

In this course, the sled motor 43 is driven and controlled by the feed servo circuit 51 so as to move a carriage composing the optical system 41 in a radial direction of the disk 40. The focus/tracking servo circuit 50 drives and controls a focus/tracking actuator (not shown in the figure) of the optical system 41 so as to perform a focus/tracking control.

The reproduction signal reproduced by the optical system 41 is supplied to the RF amplifier 49. The RF amplifier 49 amplifies the reproduction signal. A main signal of the reproduction signal is supplied to the CD encode/decode circuit 53, and is decoded by the CD encode/decode circuit 53.

The CD-ROM encode/decode circuit 57 performs

from the latch circuit 113 and the both-edge signal from the both-edge detection circuit 111. The digital LPF circuit 114 digitally performs a low pass filtering process based on the counted values supplied from the latch circuit 113 so as to cut off noise components. The frequency-modulated (FM) signal subjected to the digital filtering process is output from a terminal 117, and then is subjected to a demodulating process so as to extract information superimposed on the wobble signal.

However, noises are superimposed on the frequency-modulated signal supplied to the both-edge detection circuit 111.

The frequency-modulated signal supplied to the both-edge detection circuit 111 crosses the zero level a plurality of times due to the noises, as shown in a magnified view in the vicinity of the zero level in FIG. 5. Therefore, when the frequency-modulated signal in this state is converted into the pulse signal, unnecessary pulses occur before and after the pulse signal, as indicated by FIG. 6-(A). Due to these unnecessary pulses, a rising edge and a falling edge are detected a plurality of times, as indicated by FIG. 6-(B). Accordingly, when clocks indicated by FIG. 6-(C) are counted between the edges indicated by FIG. 6-(B), a multitude of small counted values are output in the vicinity of the zero level, as indicated by FIG. 6-(D).

Thereupon, there has been proposed a method for detecting the edges of the pulse signal ~~with~~ while excluding periods influenced by the noises. A description will be given, with reference to FIG. 7, of the method for detecting the edges of the pulse signal ~~with~~ while excluding periods influenced by the noises.

FIG. 7-(A) indicates an input pulse signal. FIG. 7-(B) indicates the pulse signal rid of influences of noises (i.e., a chattering). FIG. 7-(C) indicates a both-edge signal of the pulse signal rid of influences of noises.

switch circuit 13 ~~composes~~ forms a first charging switch circuit of the first charge circuit. The capacitor 20 composes a third capacitor of the first charge circuit. The analog switch circuit 15 composes a first discharging switch circuit of the first charge circuit. The constant current source 12, the analog switch circuit 14, the capacitor 21, the inverter circuit 37 and other elements compose a second charge circuit of the charging circuit. The constant current source 12 composes a second constant current source of the second charge circuit. The analog switch circuit 14 composes a second charging switch circuit of the second charge circuit. The capacitor 21 composes a fourth capacitor of the second charge circuit. The analog switch circuit 16 composes a second discharging switch circuit of the second charge circuit. The analog switch circuits 17 and 18, the capacitors 22 and 23, the buffer amplifiers 24 and 25 and other elements compose a sample hold circuit of the integrating means. The comparator 26 composes a first comparing circuit of the sample hold circuit. The comparator 27 composes a second comparing circuit of the sample hold circuit. The analog switch circuit 18, the capacitor 23, the buffer amplifier 25 and other elements compose a first sample hold circuit of the sample hold circuit. The analog switch circuit 18 composes a first switch circuit of the first sample hold circuit. The capacitor 23 composes a first capacitor of the first sample hold circuit. The analog switch circuit 17, the capacitor 22, the buffer amplifier 24 and other elements compose a second sample hold circuit of the sample hold circuit. The analog switch circuit 17 composes a second switch circuit of the second sample hold circuit. The capacitor 22 composes a second capacitor of the second sample hold circuit. The analog switch circuit